IN THE CLAIMS

The following claims are presented for examination.

1. (Currently Amended) An electronic circuit comprising:

a load circuit comprised of at least one field effect transistor (FET) device; ~~and~~

a headswitch comprised of at least one N-channel FET (N-FET) device and coupled between a power supply and the load circuit, wherein the headswitch is operative to couple the power supply to the load circuit when the headswitch is enabled and to cut off the power supply from the load circuit when the headswitch is disabled; and

a charge pump coupled to the headswitch, the charge pump selectively enabled based on a charge pump control signal, and operative to control the headswitch based at least in part on the charge pump control signal.

2. (Canceled)

3. (Currently Amended) The electronic circuit of claim 1~~2~~, wherein the control signal for the headswitch has a first voltage when the headswitch is enabled and a second voltage when the headswitch is disabled.

4. (Original) The electronic circuit of claim 3, wherein the first voltage is higher than a voltage of the power supply.

5. (Original) The electronic circuit of claim 3, wherein the first voltage is equal to or higher than a voltage of the power supply plus a threshold voltage of the at least one N-FET device.

6. (Original) The electronic circuit of claim 3, wherein the first voltage results in a drain to source voltage drop across the at least one N-FET device of less than a threshold voltage for the at least one N-FET device.

7. (Original) The electronic circuit of claim 1, wherein the at least one N-FET device is fabricated with a high threshold voltage.

8. (Original) The electronic circuit of claim 1, wherein the at least one N-FET device is dimensioned with a size to limit power dissipation of the headswitch to within a predetermined percent of total power of the headswitch and load circuit.

9. (Original) The electronic circuit of claim 1, wherein the headswitch comprises a plurality of N-FET devices.

10. (Currently Amended) The electronic circuit of claim 1~~2~~, further comprising:

an operational amplifier coupled to the charge pump and the headswitch in a feedback configuration to implement a linear voltage regulator.

11. (Currently Amended) The electronic circuit of claim 10, wherein the operational amplifier is operative to provide a voltage control signal for the charge pump, and wherein the voltage control signal for the charge pump maintains a load supply provided by the headswitch to the load circuit at a selected voltage.

12. (Currently Amended) The electronic circuit of claim 1~~2~~, further comprising:

an analog-to-digital converter (ADC) coupled to the headswitch; and

a controller coupled to the ADC and the charge pump, wherein the controller, charge pump, headswitch, and ADC are coupled in a feedback configuration to implement a digital voltage regulator.

13. (Original) The electronic circuit of claim 12, wherein the ADC is operative to convert a load supply voltage provided by the headswitch to the load circuit into a digital signal, wherein the controller is operative to provide a digital control for the charge pump based on the digital signal from the ADC and a digital target value, and wherein the digital control maintains a load supply provided by the headswitch to the load circuit at a selected voltage.

14. (Original) The electronic circuit of claim 13, wherein the digital target value is programmable to achieve different voltages for the load supply.

15. (Currently Amended) ~~The electronic circuit of claim 13,~~ An electronic circuit comprising:

a load circuit comprised of at least one field effect transistor (FET) device;

a headswitch comprised of at least one N-channel FET (N-FET) device and coupled between a power supply and the load circuit, wherein the headswitch is operative to couple the power supply to the load circuit when the headswitch is enabled and to cut off the power supply from the load circuit when the headswitch is disabled;

a charge pump coupled to the headswitch and operative to provide a control signal for the headswitch;

an analog-to-digital converter (ADC) coupled to the headswitch;

a controller coupled to the ADC and the charge pump, wherein the controller, charge pump, headswitch, and ADC are coupled in a feedback configuration to implement a digital voltage regulator;

wherein the ADC is operative to convert a load supply voltage provided by the headswitch to the load circuit into a digital signal, wherein the controller is operative to provide a digital control for the charge pump based on the digital signal from the ADC and a digital target value, and wherein the digital control maintains a load supply provided by the headswitch to the load circuit at a selected voltage; and

wherein the charge pump includes a plurality of stages, and wherein the digital control enables selected ones of the plurality of stages.

16. (Original) The electronic circuit of claim 1, wherein the load circuit is a microprocessor.

17. (Original) The electronic circuit of claim 1, wherein the load circuit is a digital signal processor.

18. (Original) The electronic circuit of claim 1, wherein the load circuit is a memory unit.

19. (Original) The electronic circuit of claim 1, wherein the load circuit is an analog circuit.

20. (Currently Amended) An integrated circuit comprising:

a load circuit comprised of at least one field effect transistor (FET) device; ~~and~~

a headswitch comprised of at least one N-channel FET (N-FET) device and coupled between a power supply and the load circuit, wherein the headswitch is operative to couple the power supply to the load circuit when the headswitch is enabled and to cut off the power supply from the load circuit when the headswitch is disabled; and

a charge pump coupled to the headswitch, the charge pump selectively enabled based on a charge pump control signal, and operative to control the headswitch based at least in part on the charge pump control signal.

21. (Canceled)

22. (Original) The integrated circuit of claim 20, wherein the load circuit implements a microprocessor.

23. (Original) The integrated circuit of claim 20, wherein the load circuit implements a static random access memory (SRAM).

24. (Original) The integrated circuit of claim 20, wherein the load circuit implements a digital signal processor (DSP).

25. (Currently Amended) The integrated circuit of claim 20, ~~and~~ wherein the integrated circuit is fabricated with a complementary metal oxide semiconductor (CMOS) technology of 0.13 μm or smaller.

26. (Currently Amended) A device in a communication system, comprising:

a load circuit comprised of at least one field effect transistor (FET) device; ~~and~~

a headswitch comprised of at least one N-channel FET (N-FET) device and coupled between a power supply and the load circuit, wherein the headswitch is operative to couple the power supply to the load circuit when the headswitch is enabled and to cut off the power supply from the load circuit when the headswitch is disabled; and

a charge pump coupled to the headswitch, the charge pump selectively enabled based on a charge pump control signal, and operative to control the headswitch based at least in part on the charge pump control signal.

27. (Canceled)

28. (Original) The device of claim 26, wherein the communication system is a code division multiple access (CDMA) communication system.